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=> d his full

     (FILE 'HOME' ENTERED AT 11:37:07 ON 17 NOV 2005)

     FILE 'REGISTRY' ENTERED AT 11:37:30 ON 17 NOV 2005
               E N4SI3/MF
L1           3 SEA ABB=ON  PLU=ON  N4SI3/MF
               E NI.SI/MF
L2         322 SEA ABB=ON  PLU=ON  NI.SI/MF
L3         836 SEA ABB=ON  PLU=ON  N SI/ELF
               E O2SI/MF
L4          48 SEA ABB=ON  PLU=ON  O2SI/MF
L5         385 SEA ABB=ON  PLU=ON  O.SI/MF
L6       22024 SEA ABB=ON  PLU=ON  O SI/ELF

     FILE 'CAPLUS' ENTERED AT 11:41:29 ON 17 NOV 2005
L7       98095 SEA ABB=ON  PLU=ON  TRISILICON TETRANITRIDE OR SILICON NITRIDE
               OR SIN OR SILICONITRIDE OR SI NITRIDE OR SI3N4
L8      101598 SEA ABB=ON  PLU=ON  L1 OR L2 OR L3 OR L7

L9      704149 SEA ABB=ON  PLU=ON  SILICON DIOXIDE OR SILICON OXIDE OR SILICA
               OR SIO OR SIO2
L10     841528 SEA ABB=ON  PLU=ON  L4 OR L5 OR L6 OR L9
L11    1105382 SEA ABB=ON  PLU=ON  VIA OR STUD OR PLUG OR HOLE OR APERTURE OR
               RIE OR REACTIV? ION ETCH? OR THROUGH HOLE OR SPUTTER? OR
               RECESS?
L12     239702 SEA ABB=ON  PLU=ON  PHOTO(A)(RESIST? OR MASK? OR LITHOG? OR
               ENGRAV?) OR PHOTORESIST? OR PHOTOMASK? OR PHOTOLITHO? OR
               PHOTOENGRAV? OR MASK? OR LITHOG? OR ENGRAV? OR ETCH OR BOE
L13        683 SEA ABB=ON  PLU=ON  (CAP OR GLASS?)(A)(DIE OR WAFER)
L14    1219313 SEA ABB=ON  PLU=ON  OXIDAT? OR LOCOS OR OXIDI? OR OXIDIZ?
L15     346072 SEA ABB=ON  PLU=ON  (BOTH OR MULTIPLE OR DOUBLE OR TWO OR 2 OR
               DUPLICATE OR FIRST OR SECOND OR BACK OR FRONT OR UNDER OR TOP
               OR BOTTOM)(2W)(SIDE OR SURFACE OR SUBSTRATE OR LAYER) OR
               UNDERSIDE OR BACKSIDE OR UNDERETCH? OR BOTTOM UP
L16         91 SEA ABB=ON  PLU=ON  L8 AND L10 AND L11 AND L12 AND L14 AND L15

L17          0 SEA ABB=ON  PLU=ON  L16 AND L13
L18         86 SEA ABB=ON  PLU=ON  (?LAYER? OR ?FILM OR ?COAT? OR LAMINAT? OR
               DEPOSI? OR ENCAPSUL?) AND L16
L19          2 SEA ABB=ON  PLU=ON  (PACKAG? OR (SEMICONDUCT? OR MEM)(2W)PACKAG
               ?) AND L18
               D IBIB ABS HITSTR 1-2
L20          6 SEA ABB=ON  PLU=ON  L18 AND PY>2004
L21         78 SEA ABB=ON  PLU=ON  L18 NOT (L19 OR L20)
L22         70 SEA ABB=ON  PLU=ON  L21 AND (SEMICONDUCT? OR WAFER OR IC OR
               CHIP OR MICRO CHIP OR MICROCHIP OR INTEGRATED CIRCUIT OR MEM)
L23          6 SEA ABB=ON  PLU=ON  L22 AND LOCOS
               D IBIB ABS HITSTR 1-6
L24         64 SEA ABB=ON  PLU=ON  L22 NOT L23
               D L24 TI,ABS 1-64

     FILE 'STNGUIDE' ENTERED AT 12:19:06 ON 17 NOV 2005

     FILE 'CAPLUS' ENTERED AT 12:36:09 ON 17 NOV 2005
               D L24 IBIB ABS HITSTR 14,15,24,28,43,48,49,52,55,63
L25         39 SEA ABB=ON  PLU=ON  L13 AND L8
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L26            8 SEA ABB=ON  PLU=ON  L15 AND L25
L27            8 SEA ABB=ON  PLU=ON  L26 NOT (L21 OR L19 OR L23)
                 D IBIB ABS HITSTR 1-8
L28           63 SEA ABB=ON  PLU=ON  L13 AND L15
L29           12 SEA ABB=ON  PLU=ON  L28 AND L10
L30            8 SEA ABB=ON  PLU=ON  L29 NOT (L19 OR L21 OR L23 OR L27)
                 D IBIB ABS HITSTR 1-8
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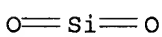
L23 ANSWER 3 OF 6 CAPLUS COPYRIGHT 2005 ACS on STN
ACCESSION NUMBER: 2002:616114 CAPLUS
DOCUMENT NUMBER: 137:178099
TITLE: Method of forming an NPN **semiconductor** device
INVENTOR(S): Kalnitsky, Alexander; Park, Sang Hoon; Scheer, Robert F.
PATENT ASSIGNEE(S): USA
SOURCE: U.S. Pat. Appl. Publ., 17 pp.
CODEN: USXXCO
DOCUMENT TYPE: Patent
LANGUAGE: English
FAMILY ACC. NUM. COUNT: 1
PATENT INFORMATION:

PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
US 2002109208	A1	20020815	US 2001-782820	20010212
US 6492237	B2	20021210		
PRIORITY APPLN. INFO.:			US 2001-782820	20010212

AB This invention relates generally to **semiconductor** processing, and in particular, to a method of forming an NPN **semiconductor** device using an oxide-nitride-oxide (ONO) **layers** for emitter formation and another implementation using a local **oxidn**. of silicon (**LOCOS**) for emitter formation. The method of forming an NPN **semiconductor** device includes the steps of forming a collector region within a substrate, forming a base region over the collector region, and forming an oxide-nitride-oxide stack over the base region. Once these 3 structures are formed, an opening is created through the oxide-nitride-oxide stack to expose the **top surface** of the base region. Then, a doped polysilicon material is used to fill the opening and make elec. contact to the base region. The use of the oxide-nitride-oxide stack with appropriate etching of the opening eliminates the exposure of the base region to **reactive ion etch** environment typical of prior art methods for forming NPN **semiconductor** devices. As an option, after the opening of the oxide-nitride-oxide stack is formed, a local **oxidn**. of Si (**LOCOS**) and etched can be preformed to create oxide spacers to line the opening wall above the base region.

IT **7631-86-9**, **Silica**, uses **12033-89-5**, **Silicon nitride**, uses
RL: DEV (Device component use); USES (Uses)
(method of forming NPN **semiconductor** device)

RN 7631-86-9 CAPLUS
CN Silica (6CI, 7CI, 8CI, 9CI) (CA INDEX NAME)



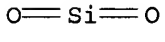
RN 12033-89-5 CAPLUS
CN Silicon nitride (Si3N4) (8CI, 9CI) (CA INDEX NAME)

L23 ANSWER 5 OF 6 CAPLUS COPYRIGHT 2005 ACS on STN
ACCESSION NUMBER: 2000:727226 CAPLUS
DOCUMENT NUMBER: 134:35458
TITLE: A fabrication process for integrating polysilicon microstructures with post-processed CMOS circuits
AUTHOR(S): Gianchandani, Y. B.; Kim, H.; Shinn, M.; Ha, B.; Lee, B.; Najafi, K.; Song, C.
CORPORATE SOURCE: Department of Electrical and Computer Engineering, University of Wisconsin, WI, 53706-1691, USA
SOURCE: Journal of Micromechanics and Microengineering (2000), 10(3), 380-386
CODEN: JMMIEZ; ISSN: 0960-1317
PUBLISHER: Institute of Physics Publishing
DOCUMENT TYPE: Journal
LANGUAGE: English

AB A **MEMS**-first fabrication process for integrating CMOS circuits with polysilicon micromech. structures is described in detail. The overall process uses 18 **masks** (22 **lithog**. steps) to merge a p-well **LOCOS** CMOS process that has one metal and **two** polysilicon **layers** with a surface micromachining process that has three **layers** of polysilicon. The microstructures are formed within **recesses** on the surface of silicon **wafers** such that their uppermost surfaces are coplanar with the remainder of the substrate. No special planarization technique, such as chemical-mech. polishing, is used in the work described here. Special aspects of the process include provisions to improve **lithog**. within the **recesses**, to protect the microstructures during the circuit fabrication, and to implement an effective lead transfer between the microstructures and the on-**chip** circuitry. The process is validated using a test vehicle that includes accelerometers and gyroscopes interfaced with sensing circuits. Measured transistor parameters match those obtained in standard CMOS, with NMOS and PMOS thresholds at 0.76 V and -0.96 V, resp.

IT **7631-86-9**, **Silica**, uses **12033-89-5**, **Silicon nitride**, uses
RL: DEV (Device component use); USES (Uses)
(fabrication process for integrating polysilicon microstructures with post-processed CMOS circuits)

RN 7631-86-9 CAPLUS
CN Silica (6CI, 7CI, 8CI, 9CI) (CA INDEX NAME)



RN 12033-89-5 CAPLUS
CN Silicon nitride (Si3N4) (8CI, 9CI) (CA INDEX NAME)

L24 ANSWER 48 OF 64 CAPLUS COPYRIGHT 2005 ACS on STN
ACCESSION NUMBER: 1999:468152 CAPLUS
DOCUMENT NUMBER: 131:94690
TITLE: Method of fabricating a microwave inductor
INVENTOR(S): Chuang, Kuen-joung; Lui, Hon-sung; Liaw, Wen-ruey
PATENT ASSIGNEE(S): Taiwan Semiconductor Manufacturing Co., Ltd., Taiwan
SOURCE: U.S., 8 pp.
CODEN: USXXAM
DOCUMENT TYPE: Patent
LANGUAGE: English
FAMILY ACC. NUM. COUNT: 1
PATENT INFORMATION:

PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
US 5930637	A	19990727	US 1997-961696	19971031
PRIORITY APPLN. INFO.:			US 1997-961696	19971031

AB Isolation regions are formed on a **top surface** of a **wafer**. An ion implantation was performed to implant ions into the **wafer**. Then, an thermal anneal process was used to form an implanted **layer** on the **wafer**. Then, a **SiO2** or **Si nitride layer** is **deposited** on the implanted **layer**. Next, a micro inductor is patterned on the insulator **layer**. Subsequently, a dielec. **layer** is formed on the inductor for isolation. Next, **via holes** are created by etching the dielec. **layer**. A conductive **layer** is patterned on the dielec. **layer** and refilled into the **via holes**. Next, a passivation **layer** is **deposited** on the dielec. **layer** and the conductive **layer**. An etching was performed to **etch** the **wafer** from a **bottom surface** (a 2nd surface) of the **wafer**. Finally, a ground plate is connected to the **bottom surface** (2nd **surface**) of the **wafer**.

IT **7631-86-9**, **Silica**, uses **12033-89-5**, **Silicon nitride**, uses
RL: DEV (Device component use); PEP (Physical, engineering or chemical process); PROC (Process); USES (Uses)
(in method of fabricating microwave inductor)

RN 7631-86-9 CAPLUS
CN Silica (6CI, 7CI, 8CI, 9CI) (CA INDEX NAME)

O=Si=O

RN 12033-89-5 CAPLUS
CN Silicon nitride (Si3N4) (8CI, 9CI) (CA INDEX NAME)

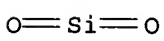
*** STRUCTURE DIAGRAM IS NOT AVAILABLE ***
REFERENCE COUNT: 2 THERE ARE 2 CITED REFERENCES AVAILABLE FOR THIS RECORD. ALL CITATIONS AVAILABLE IN THE RE FORMAT

L24 ANSWER 55 OF 64 CAPLUS COPYRIGHT 2005 ACS on STN
ACCESSION NUMBER: 1993:92578 CAPLUS
DOCUMENT NUMBER: 118:92578
TITLE: Manufacture of dynamic random-access memories
INVENTOR(S): Doi, Tsukasa
PATENT ASSIGNEE(S): Sharp Corp., Japan
SOURCE: Jpn. Kokai Tokkyo Koho, 5 pp.
CODEN: JKXXAF
DOCUMENT TYPE: Patent
LANGUAGE: Japanese
FAMILY ACC. NUM. COUNT: 1
PATENT INFORMATION:

PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
JP 04214666	A2	19920805	JP 1990-401637	19901212
JP 2633395	B2	19970723		
PRIORITY APPLN. INFO.:			JP 1990-401637	19901212

AB The process includes (a) forming an **interlayer** insulator **film** on the transistor formed on a **semiconductor** substrate; (b) **depositing** a **Si3N4 film** on the insulator **film**, thermally **oxidizing** its surface; (c) forming a **SiO2 film**, which has a wave-like surface, by normal-pressure chemical vapor **deposition** on the **Si3N4 film** using tetra-ethoxy silane and O2; (d) forming a contact **hole** in the **laminate** of the **interlayer** insulator **film**, the **Si3N4 film**, and the **SiO2 film** on the source region of the transistor; (e) decreased-pressure chemical vapor **deposition** of a uniformly thick poly-Si **film**, and patterning it to form an electrode which is connected with the source region through the contact **hole**, and which extends over the transistor, reflecting the wave-like shape of the **SiO2 film**; (f) **etch** removal of both the **SiO2** and **Si3N4** films, or only the **SiO2 film**, so that the part of the electrode, which extends over, the transistor, protrudes from the substrate, while the electrode bottom does not contact the substrate; (g) forming a capacitor insulator **film** which covers the **top**, **side**, and **bottom surfaces** of the electrode; and (h) forming another electrode facing the **top**, **side**, and **bottom surfaces** of the electrode. The dynamic RAM has increased charge-storage capacitance.

IT **7631-86-9**, **Silicon oxide (SiO2)**, uses **12033-89-5**, **Silicon nitride (Si3N4)**, preparation
RL: PEP (Physical, engineering or chemical process); PROC (Process)
(chemical vapor **deposition** of, in manufacture of dynamic RAMs)
RN 7631-86-9 CAPLUS
CN Silica (6CI, 7CI, 8CI, 9CI) (CA INDEX NAME)



RN 12033-89-5 CAPLUS
CN Silicon nitride (Si3N4) (8CI, 9CI) (CA INDEX NAME)

L24 ANSWER 63 OF 64 CAPLUS COPYRIGHT 2005 ACS on STN
ACCESSION NUMBER: 1971:513874 CAPLUS
DOCUMENT NUMBER: 75:113874
TITLE: Local **oxidation** of silicon; new technological aspects
AUTHOR(S): Appels, J. A.; Paffen, M. M.
CORPORATE SOURCE: Neth.
SOURCE: Philips Research Reports (1971), 26(3), 157-65
CODEN: PRREA9; ISSN: 0031-7918
DOCUMENT TYPE: Journal
LANGUAGE: English

AB Partly or fully countersunk thick **SiO2** patterns were prepared on Si by local **oxidn**. Starting with a thin 1500-Å pattern of **Si3N4**, different structures were obtained by (i) direct **oxidn**., which yielded half-**recessed** oxide patterns; (ii) preliminary Si etching before **oxidn**., which gave a completely countersunk oxide pattern; and (iii) more pronounced mesa etching and subsequent **oxidn**., which resulted in a mesa structure with oxide on the flanks only. When **SiO2**-**Si3N4** sandwich structures were used for **masking**, the edge of the **oxidized** pattern was less abrupt than in the case of **Si3N4** only. In another method, the combination of local **oxidn**. and diffusion made use of controlled **underetching** of **Si3N4** -**SiO2** sandwich structures to produce well-defined diffused regions under countersunk oxide patterns.

IT **7631-86-9**, uses and miscellaneous
RL: DEV (Device component use); TEM (Technical or engineered material use); USES (Uses)
(**coatings**, in **semiconductor** devices, local **oxidn**. of silicon for)
RN 7631-86-9 CAPLUS
CN Silica (6CI, 7CI, 8CI, 9CI) (CA INDEX NAME)

O=Si=O

L27 ANSWER 1 OF 8 CAPLUS COPYRIGHT 2005 ACS on STN
ACCESSION NUMBER: 2004:394700 CAPLUS
DOCUMENT NUMBER: 142:327231
TITLE: Incrementally etched electrical feedthroughs for wafer-level transfer of glass lid packages
AUTHOR(S): Oberhammer, Joachim; Stemme, Goeran
CORPORATE SOURCE: Dept. of Signals, Sensors and Systems, Royal Institute of Technology, Stockholm, 100 44, Swed.
SOURCE: Transducers '03, International Conference on Solid-State Sensors, Actuators and Microsystems, Digest of Technical Papers, 12th, Boston, MA, United States, June 8-12, 2003 (2003), Volume 2, 1832-1835. Institute of Electrical and Electronics Engineers: New York, N. Y.
CODEN: 69FHV2; ISBN: 0-7803-7731-1
DOCUMENT TYPE: Conference
LANGUAGE: English
AB This paper reports on a simple fabrication technique to create full wafer-level transferred glass-lid encapsulations for near-hermetic packaging of MEMS devices using adhesive wafer bonding with Benzocyclobutene. Also, a new technique to create low-d. feedthroughs through the **glass wafer** for elec. interconnections from the back to the **front side** of the glass-lids is introduced. The through-wafer vias are fabricated by combining a mech. etch-step by powder-blasting from the **back side** and a subsequent short HF wet etch step. The advantage of this via technique is that the major part of the via is etched without going completely through the wafer, allowing standard surface micromachining processes on the **front side** of the **glass wafer** before the final opening of the via.
IT **12033-89-5**, **Silicon nitride**, processes
RL: DEV (Device component use); PEP (Physical, engineering or chemical process); PYP (Physical process); PROC (Process); USES (Uses)
(incrementally etched elec. feedthroughs for wafer-level transfer of glass lid packages of MEMS)
RN 12033-89-5 CAPLUS
CN Silicon nitride (Si3N4) (8CI, 9CI) (CA INDEX NAME)

*** STRUCTURE DIAGRAM IS NOT AVAILABLE ***
REFERENCE COUNT: 10 THERE ARE 10 CITED REFERENCES AVAILABLE FOR THIS RECORD. ALL CITATIONS AVAILABLE IN THE RE FORMAT

11/17/2005 10/708936 Doty

File 2:INSPEC 1898-2005/Nov W1
(c) 2005 Institution of Electrical Engineers

Set	Items	Description
S1	9379	E3,E5,E7
S2	15394	CI=(SI BIN(S)N BIN)
S3	75071	CI=SIO2
S4	60571	CI=(SI BIN(S)O BIN)
S5	25050	TRISILICON? ?()TETRA()NITRIDE? ? OR SILICON()NITRIDE OR SIN OR SILICONITRIDE OR SI()NITRIDE OR SI3N4
S6	1349384	VIA? ? OR STUD? ? OR PLUG? ? OR HOLE? ? OR APERTURE? ? OR RIE OR REACTIVE()ION()ETCH????? OR THROUGH()HOLE OR RECESS????
S7	934031	SEMICONDUCT????? OR WAFER OR IC OR SEMI()CONDUCT????? OR CHIP OR MICRO()CHIP OR MICROCHIP OR INTEGRATE?????()CIRCUIT???
S8	136255	PHOTO()(RESIST????? OR MASK??? OR LITHOG????? OR ENGRAV???-?) OR PHOTORESIST???? OR PHOTOMASK????? OR PHOTOLITHO????? OR PHOTOENGRAV???? OR MASK???? OR LITHOG????? OR ENGRAV???? OR ETCH????? OR BOE
S9	247697	OXIDAT????? OR LOCOS OR OXIDIS????? OR OXIDIZ??? OR OXID??-???????
S10	125390	(BOTH OR DUAL OR MULTIPLE OR DOUBLE OR TWO OR 2 OR DUPLICATE OR FIRST OR SECOND)(2W)(SIDE??? OR SURFACE??? OR SUBSTRATE-??? OR LAYER???)
S11	31535	S1 OR S2 OR S5
S12	131038	S3 OR S4 OR (DIOXOSILICON OR SILICON()DIOXIDE OR SILICON()-OXIDE OR SILICA OR SIO OR SIO2)
S13	9	S11 AND S12 AND S6 AND S7 AND S8 AND S9 AND S10
S14	362	(CAP????? OR GLASS???)()(DIE???? OR WAFER???)
S15	0	S11 AND S12 AND S6 AND S8 AND S9 AND S14
S16	134	S11 AND S12 AND S6 AND S8 AND S9
S17	134	S16 AND S9
S18	1089003	LAYER????? OR FILM???? OR COAT????? OR OVERCOAT????? OR DEPOSI?????? OR ENCAPSUL??????
S19	110	S17 AND S18
S20	144457	PACKAG????? OR SEMICONDUCT??????(2W)PACKAG????? OR DIE? ?
S21	4	S19 AND S20
S22	4	S21 NOT S13
S23	0	S11 AND S6 AND S8 AND S9 AND S14
S24	1	S14 AND S6 AND S8 AND S9 AND S10
S25	1	S24 NOT (S13 OR S22)
S26	84	S14 AND S6
S27	43	S26 AND S8
S28	2	S27 AND S9
S29	1	S28 NOT(S13 OR S22 OR S25)
S30	4	S27 AND S11
S31	4	S30 NOT (S13 OR S22 OR S25 OR S29)
S32	4	S27 AND S11
S33	0	S32 NOT (S13 OR S22 OR S25 OR S29 OR S31)
S34	8	S27 AND S10
S35	5	S34 NOT(S13 OR S22 OR S25 OR S29 OR S31)
S36	19	S27 AND S18
S37	12	S36 NOT(S13 OR S22 OR S25 OR S29 OR S31 OR S35)

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EIC 2800 MARY S. MIMS 272-5928